CLAIMS

I claim:

1. A method for making a deep trench in a silicon layer, comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a plasma gas comprising a Cl_2, HBr, O_2, and Ar; and

removing the patterned mask.

2. The method of claim 1, wherein the deep trench has a depth ranging from about 1.25 microns to about 20 microns.

3. The method of claim 1, wherein the deep trench has a depth ranging from about 1.5 microns to about 5 microns.

4. A method for making a trench in a silicon layer, comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a uniform plasma gas comprising a chlorine-containing gas, a passivating gas, a selectivity gas, and a diluent gas; and

removing the patterned mask.

5. The method of claim 4, wherein the chlorine-containing gas comprises Cl_2.

6. The method of claim 4, wherein the passivating gas comprises HBr.

7. The method of claim 4, wherein the selectivity gas is O_2.

8. The method of claim 4, wherein the diluent gas is Ar.

9. The method of claim 4, wherein the uniform gas plasma etches a plurality of trenches with a substantially uniform depth.

10. The method of claim 4, wherein the etching is performed in a single step.

11. A method for making a plurality of trenches in silicon layer, comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a depth uniformity of less than about 2 %.

12. The method of claim 11, wherein the depth uniformity is less than about 0.5 %.

13. The method of claim 11, wherein the variance in trench depth is less than about 500 angstroms.

14. The method of claim 11, wherein the variance in trench depth ranges from about 50 to about 500 angstroms.

15. The method of claim 11, wherein the depth uniformity is independent of the width of the plurality of trenches.

16. A method for making a plurality of trenches in silicon layer, comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a sidewall angle uniformity of less than about 0.5%.

17. The method of claim 16, wherein the plurality of trenches has substantially the same sidewall angle.

18. The method of claim 16, wherein the sidewall angle uniformity of less than about 0.15%.

19. The method of claim 16, wherein the sidewall angle is about 89°.

20. A method for making a plurality of trenches in a silicon layer, comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a uniform plasma gas comprising a Cl_2, HBr, O_2, and Ar; and

removing the patterned mask;

the plurality of trenches having a depth ranging from about 1.5 to about 25 microns and a depth uniformity of less than about 2 %.

21. A method for making a semiconductor device containing a deep trench in a silicon layer, comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a plasma gas comprising a Cl_2, HBr, O_2, and Ar; and removing the patterned mask.

22. A method for making a semiconductor device containing a trench in a silicon layer, comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a uniform plasma gas comprising a chlorine-containing gas, a passivating gas, a selectivity gas, and a diluent gas; and

removing the patterned mask.

23. A method for making a semiconductor device containing a plurality of trenches in a silicon layer, comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a depth uniformity of less than about 2 %.

24. A method for making semiconductor device containing a plurality of trenches in a silicon layer, comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a sidewall angle uniformity of less than about 0.5%.

25. A deep trench in a silicon layer made by the method comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a plasma gas comprising a Cl_2, HBr, O_2, and Ar; and

removing the patterned mask.

26. A trench in a silicon layer made by the method comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a uniform plasma gas comprising a chlorine-containing gas, a passivating gas, a selectivity gas, and a diluent gas; and

removing the patterned mask.

27. A plurality of trenches in a silicon layer made by the method comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a depth uniformity of less than about 2 %.

28. A plurality of trenches in a silicon layer made by the method comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a sidewall angle uniformity of less than about 0.5 %.

29. A semiconductor device containing a deep trench in a silicon layer made by the method comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a plasma gas comprising a Cl_2, HBr, O_2, and Ar; and removing the patterned mask.

30. A semiconductor device containing a trench in a silicon layer made by the method comprising:

providing a silicon layer;

providing a patterned mask over the silicon layer;

etching the silicon layer with a uniform plasma gas comprising a chlorine-containing gas, a passivating gas, a selectivity gas, and a diluent gas; and

removing the patterned mask.

31. A semiconductor device containing a plurality of trenches in a silicon layer made by the method comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a depth uniformity of less than about 2 %.

32. A semiconductor device containing a plurality of trenches in a silicon layer made by the method comprising:

providing a silicon layer;

providing a mask over the silicon layer;

etching the silicon layer with a gas mixture comprising a chlorine-containing gas to make a plurality of trenches; and

removing the patterned mask;

the plurality of trenches having a sidewall angle uniformity of less than about 0.5 %.

33. A silicon layer containing a plurality of trenches, wherein the plurality of trenches has a depth uniformity of less than about 2%.

34. The silicon layer of claim 33, wherein the variance in trench depths is up to about 500 angstroms.

35. The silicon layer of claim 33, wherein the depth uniformity is independent of the width of the plurality of trenches.

36. A silicon layer containing a plurality trenches, wherein the plurality of trenches has a sidewall angle uniformity of less than about 0.5%.

37. The silicon layer of claim 36, wherein the plurality of trenches has substantially the same sidewall angle.

38. A plurality of trenches in a silicon layer, wherein the plurality of trenches has a depth uniformity of less than about 2%.

39. The plurality of trenches of claim 38, wherein the variance in trench depths is up to about 500 angstroms.

40. The plurality of trenches of claim 38, wherein the depth uniformity is independent of the width of the plurality of trenches.

41. A plurality of trenches in a silicon layer, wherein the plurality of trenches has a sidewall angle uniformity of less than about 0.5%.

42. The plurality of trenches of claim 41, wherein the plurality of trenches has substantially the same sidewall angle.

43. A semiconductor device containing plurality of trenches in a silicon layer, wherein the plurality of trenches has a depth uniformity of less than about 2%.

44. The semiconductor device of claim 43, wherein the variance in trench depths is up to about 500 angstroms.

45. The semiconductor device of claim 43, wherein the depth uniformity is independent of the width of the plurality of trenches.

46. A semiconductor device containing plurality of trenches in a silicon layer, wherein the plurality of trenches has a sidewall angle uniformity of less than about 0.5%.

47. The semiconductor device of claim 41, wherein the plurality of trenches has substantially the same sidewall angle.

48. A semiconductor device containing plurality of vertical transistors in a silicon layer, wherein the plurality of vertical transistors has a depth uniformity of less than about 2%.

49. A semiconductor device containing plurality of vertical transistors in a silicon layer, wherein the plurality of vertical transistors has a sidewall angle uniformity of less than about 0.5%.

50. A plurality of vertical transistors in a silicon layer, wherein the plurality of transistors has a depth uniformity of less than about 2%.

51. A plurality of vertical transistors in a silicon layer, wherein the plurality of transistors has a sidewall angle uniformity of less than about 0.5%.